Curriculum for
Master of Technology
in
VLSI & Embedded Systems

(MTech VLSI & ES)

(Pattern 2024)

With Effect From A.Y. 2024-25

Matoshri Education Society's

Matoshri College of Engineering and Research Centre, Eklahare, Nashik (Autonomous)

NBA and NAAC Accredited, Approved by All India Council for Technical Education, New Delhi, Affiliated to Savitribai Phule Pune University, College Code:5177

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Eklahare shivar, Near Odhagaon, Off Nashik-Aurangabad Highway, Nashik, Maharashtra 422105

Curriculum for Post Graduate Programme- MTech VLSI & ES
(Pattern 2024)

Matoshri College of Engineering and Research Centre, Eklahare, Nashik has been granted the academic autonomous status from academic year 2024-25 by University Grant Commission. The Academic autonomous status has been considered as an opportunity for imparting comprehensive education. The academic autonomous status can be utilized to implement the National Education Policy (NEP 2020) effectively. The institute has a prudent plan to incorporate necessary dynamism in academic structure to march towards the vision of the institute and develop the research and skill oriented human resources contributing to the development of the nation.

With a focus on staying at the forefront of educational innovation, the institution diligently prepares curricula that are both dynamic and industry-aligned. This process entails meticulous planning and collaboration to ensure the development of comprehensive programs catering to the evolving needs of students and industries alike.

The highlights of Master of Technology (MTech) curriculum:

- Every Post Graduate programme is of two years duration with four semesters.
- The curricula have been designed adhering to the NEP guidelines and norms.
- Efforts have been taken to design the curricula which are unambiguous and self-explanatory.
- Students have to earn 84 credits for the award of MTech degree.

Credit Requirement and Eligibility for the PG Programme

Eligibility first year PG admissions will be as per guidelines provided by Admission Regulating Authority of Government of Maharashtra and guidelines of NEP2020.

Examination and Passing

Rules of Passing

- To pass the course, the student has to earn a minimum of 40 percent marks in End Semester exam and 40 percent average marks(In-Semester marks + End-Semester marks) in the exam head.
- Students can earn the credit of the course if he/she passes the course with appropriate grade.
- The student is declared as PASS in the corresponding year if he/she earns the credits of all the courses of the year.
- A student will be awarded the master's degree if he/she earns 84 credits.

Rules of A.T.K.T.

The students who is not detained to appear in examination either in first semester or second semester of First year and, has filled the form of examination is eligible to take admission in second year of PG course.

Exit Point:

For those who join 2 year PG programmes, there shall only be one exit point. Students who exit at the end of 1st year shall be awarded a Postgraduate Diploma.

This document includes-

- Credit Distribution Across Semesters and Course Code Nomenclature
- Examination Heads and Assessment Schemes
- Various Courses' Categories, Description and Abbreviation
- Program Outcomes
- Four Semesters Course Structures
- Broad Courses' Categories, and Credit Distribution
- Curriculum for semester I
- Curriculum for semester II
- Curriculum for semester III
- Curriculum for semester IV

Matoshri College of Engineering and Research Centre (Autonomous)
Curriculum for
Master of Technology in VLSI & Embedded Systems (MTech VLSI & ES) 2024-25

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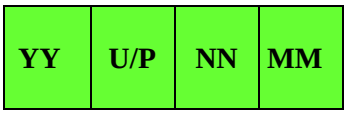
Table 1: Total Credits and Total Marks for Master of Technology (MTech VLSI & ES)		
Semester	**Total Credits**	**Total Marks**
I	22	650
II	22	650
III	20	600
IV	20	600
Total	**84**	**2500**

Table 2: Nomenclature for Course Codes

Format for Course Codes-
YY - Year of Course launch
U/P- **U** : Undergraduate ; **P**: Postgraduate
NN- Branch Code
MM- Course Number



NN	Post Graduate Programme	NN	Post Graduate Programme
10	MTech Geotechnical Engineering	13	MTech Electrical Power Systems
11	MTech Data Science	14	MTech Heat Power Engineering
12	MTech VLSI and Embedded Systems	15	Master of Computer Applications (MCA)

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Table 3: Examination Heads and Assessment Schemes

Exam Head	Abbreviation	In Semester Exam (40% of Total Marks)		End Semester Exam (60% of Total Marks)
		In_Sem_Exam_1 (20%)	In_Sem_Exam_2 (20%)	
Theory	**TH**	CAT/CCE based on 20% curriculum	CAT/CCE based on 20% curriculum	Theory examination based on 60% curriculum
Project	**PROJ**	Progress Review I with Demonstration, Presentation, Oral & Report	Progress Review II with Demonstration, Presentation, Oral & Report	Activity, Presentation, Demonstration, Oral & Report as applicable
Internship	**INT**	Progress Review I with Activity, Presentation, Demonstration, Oral & Report as applicable	Progress Review II with Activity, Presentation, Demonstration, Oral & Report as applicable	Activity, Presentation, Demonstration, Oral & Report as applicable
Practical	**PR**	Mid-semester exam based on experiment/ activity performance, demonstration, Presentation, Oral and Journal, Report as applicable		Experiment, activity performance, demonstration, Presentation, Oral & Report, journal as applicable
Term work	**TW**	Mid-semester exam based on experiment/ activity performance, demonstration, Presentation, Oral and Journal, Report as applicable		Activity, Experiment performance, demonstration, Presentation, Oral & Report, journal as applicable
Seminar	**SEMI**	Mid-semester review based on topic of study, literature study, draft of paper manuscript, report(s) and other as applicable		Discussions, Presentation, Report(s), publication as applicable
Continuous Assessment Test	**CAT**	Class test examination to assess and evaluate a student's progress with descriptive or objective questions as measure of the student's knowledge and skills in online or offline mode.		
Continuous and Comprehensive Evaluation	**CCE**	Examination that evaluate learners' abilities based on various dimensions viz- academic performance, work experience, skills, coordination, agility, innovation, teamwork, public speaking, behavior, and similar as a measure of knowledge, skills and attitude.		

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Table 4: Various Courses' Categories, Description and Abbreviation		
Broad Category	**Description**	**Abbreviations**
Program Courses	Programme Core Course	PCC
	Programme Core Course Lab	PCCL
	Programme Elective Course	PEC
	Programme Elective Course Lab	PECL
Multidisciplinary Courses	Multidisciplinary Course	MDC
	Generic Elective	GE
Experiential Learning Courses	Project	PROJ
	Internship / On Job Training	INT / OJT
Course Type/ Teaching Learning Schemes / Examination Heads	Practical	PR
	Internship	INT
	Theory	TH
	Tutorial	TUT
	Lecture	Lect
	Laboratory Course	Lab
	Term work	TW
	Seminar	SEMI
MOOC	Massive Open Online Courses by NPTEL under SWAYAM	MOOC
Project Management, Finance and Governance	Project Planning/ Entrepreneurship Development / Engineering Economics / Management/ Corporate Laws/ Corporate Governance	PMFG
In Semester Examination	In_Sem_Exam	ISE
Continuous Assessment Test	Continuous Assessment Test	CAT
End Semester Examination	End_Sem_Exam	ESE
Continuous & Comprehensive Evaluation	Continuous & Comprehensive Evaluation	CCE
Bloom's Taxonomy	Bloom's Taxonomy	BL
Course Outcome	Course Outcome	CO
Program Outcome	Program Outcome	PO

Table 5: Program Outcomes At the end of Post Graduate Program, a student would have:	
PO1	**Problem Solving and Research Skill:** An ability to independently carry out research /investigation and development work to solve practical problems
PO2	**Communication:** An ability to write and present a substantial technical report/document
PO3	**Lifelong Learning:** Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program
PO4	**Critical Thinking, Project Management and Finance, Scholarship of knowledge:** Demonstrate advanced knowledge and skills understanding management principle to analyze complex engineering problems critically, and apply the same to, manage projects efficiently in respective disciplines and multidisciplinary environments after consideration of economical and financial factors while working as individual or in teams or as a leader in a team
PO5	**Collaborative and Multidisciplinary work:** An ability to think critically and apply appropriate logic, analysis, judgment and decision making and to function as an effective member or leader of engineering teams to achieve common goals
PO6	**Usage of Modern Tools, Ethical Practices and Social Responsibility:** An ability to use appropriate techniques, skills, and modern engineering tools necessary for engineering practice and commit to professional ethics and responsibilities

Program Specific Outcomes At the end of Post Graduate Program,	
PSO1:	**Design and create novel systems** in the field of VLSI design technology and embedded electronic systems to address and solve global challenges contributing to advancements in technology and society.
PSO2:	**Carry out research activities** in Electronics, VLSI design and technology using advanced hardware and software tools specific to the field, contributing to innovations and advancements in the industry.

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Matoshri College of Engineering and Research Centre, Eklahare, Nashik

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Table 6: First Year of MTech (FY MTech VLSI & ES)

Semester I

Courses				Teaching Scheme Hrs/Week			Examination and Marks (% of Total Curriculum and Marks)				Credit			
							In_Sem Exam (40%)		End_Sem Exam (60%)	Marks				
Course Code	Course Type	Title of Course	Exam Head	Lect	TUT	PR	CAT	CCE	ESE	Total	TH	TUT	PR	Total
24P1201	MDC	Physics of VLSI Devices	TH	04	-	-	20	20	60	100	04	-	-	04
24P1202	PCC	MOOC_1 #	TH	04	-	-	20	20	60	100	04	-	-	04
24P1203	PCC	Research Methodology	TH	02	-	-	20	20	60	100	02	-	-	02
24P1204	PCC	Embedded System Design	TH	04	-	-	20	20	60	100	04	-	-	04
24P1205	PEC	Program Elective Course_1	TH	04	-	-	20	20	60	100	04	-	-	04
24P1206	PCCL	Digital design and Embedded system Lab	PR	-	-	04	20		30	50	-	-	02	02
24P1207	PECL	Elective 1 Lab	PR	-	-	02	20		30	50	-	-	01	01
24P1208	PMFG	Study of Indian Constitution	SEMI	-	01	-	20		30	50	-	01		01
Total				**18**	**01**	**06**	**260**		**390**	**650**	**18**	**01**	**03**	**22**
Total Hours/ Week				**25**			**650**				**22**			

Program Elective Course_1	
Course Code	**Course Name**
24P1205-A	Micro Electromechanical Systems
24P1205-B	VLSI Digital Signal Processing
24P1205-C	Low Power IC Design
24P1205-D	System Design with FPGA
24P1205-E	Generic Elective **

MOOC_1: NPTEL Courses under SWAYAM for AY 2024-25	
Course Code	**Course Name^**
24P1202-A	Microelectronics: Devices to Circuits
24P1202-B	CAD for VLSI Design II
24P1202-C	System Design Through Verilog
24P1202-D	Digital VLSI Testing

^**Note:** Course Names will be declared as per availability of NPTEL courses of 12/16 weeks in that particular year for the semester.

****GE:** An elective course chosen generally from an unrelated discipline/subject, with an intention to seek knowledge beyond the discipline. A core course offered in a discipline/subject may be treated as an elective by other discipline/subject and vice versa.

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Table 7: First Year of MTech (FY MTech VLSI & ES)
Semester II

Courses				Teaching Scheme Hrs/Week			Examination and Marks (% of Total Curriculum and Marks)				Credit			
							In_Sem Exam (40%)		End_Sem Exam (60%)	Marks				
Course Code	Course Type	Title of Course	Exam Head	Lect	TUT	PR	CAT	CCE	ESE	Total	TH	TUT	PR	Total
24P1209	PCC/ MDC	MOOC_2	TH	04	-	-	20	20	60	100	04	-	-	04
24P1210	PCC	Analog IC Design	TH	04	-	-	20	20	60	100	04	-	-	04
24P1211	PCC	ASIC Design	TH	04	-	-	20	20	60	100	04	-	-	04
24P1212	PEC	Program Elective Course_2	TH	04	-	-	20	20	60	100	04	-	-	04
24P1213	PCCL	Analog IC and ASIC Design Lab	TW+ PR	-	-	04	40		60	100	-		02	02
24P1214	PECL	Elective_2 Lab	TW+ PR	-	-	04	40		60	100	-	-	02	02
24P1215	PMFG	Project and Finance Management	SEMI	-	01	02	20		30	50	-	01	01	02
Total				**16**	**01**	**10**	**260**		**390**	**650**	**16**	**01**	**05**	**22**
Total Hours/ Week				**27**			**650**				**22**			

Program Elective Course_2	
Course Code	**Course Name**
24P1212-A	Micro Sensors and Interface Electronics
24P1212-B	System-on-Chip Design
24P1212-C	Mixed Signal IC Design
24P1212-D	Real Time Operating Systems
24P1212-E	Generic Elective **

MOOC_2: NPTEL Courses under SWAYAM for AY 2024-25	
Course Code	**Course Name^**
24P1209-A	Analog IC Design
24P1209-B	Advanced VLSI Design
24P1209-C	VLSI Technology
24P1209-D	Advance Digital Signal Processing

^**Note:** Course Names will be declared as per availability of NPTEL courses of 12/16 weeks in that particular year for the semester.

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Matoshri College of Engineering and Research Centre, Eklahare, Nashik

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Table 8: Second Year of MTech (FY MTech VLSI & ES)
Semester III

Courses				Teaching Scheme Hrs/Week			Examination and Marks (% of Total Curriculum and Marks)				Credit			
							In_Sem Exam (40%)		End_Sem Exam (60%)	Marks				
Course Code	Course Type	Title of Course	Exam Head	Lect	TUT	PR	CCE_1	CCE_2	ESE	Total	TH	TUT	PR	Total
24P1216	PCC	MOOC_3	TH	04	-	-	20	20	60	100	04	-	-	04
24P1217	PCC	VLSI Testing and Testability	TH	04	-	-	20	20	60	100	04	-	-	04
24P1218	PEC	Program Elective Course -3	TH	04	-	-	20	20	60	100	04	-	-	04
24P1219	PCCL	VLSI Testing and Testability Lab	PR	-	-	02	20		30	50	-	-	01	01
24P1220	PMFG	Company Law and Corporate Governance	SEMI	-	01	-	20		30	50	-	01	-	01
24P1221	PROJ	Dissertation Stage-I	PROJ	-	-	12	40	40	120	200	-	-	06	06
Total				**12**	**01**	**14**	**240**		**360**	**600**	**12**	**01**	**07**	**20**
Total Hours/ Week				**27**			**600**				**20**			

Program Elective Course_3	
Course Code	**Course Name**
24P1218-A	RFIC Design
24P1218-B	DSP Architectures
24P1218-C	Bio Sensors and Circuits
24P1218-D	High Speed ICs
24P1218-E	Generic Elective **

MOOC_3: NPTEL Courses under SWAYAM for AY 2025-26	
Course Code	**Course Name^**
24P1216-A	Analog VLSI Design
24P1216-B	VLSI Design Flow: RTL to GDS
24P1216-C	Microelectronics: Devices to Circuits
24P1216-D	VLSI Interconnects

^**Note:** Course Names will be declared as per availability of NPTEL courses of 12/16 weeks in that particular year for the semester.

****GE:** An elective course chosen generally from an unrelated discipline/subject, with an intention to seek knowledge beyond the discipline. A core course offered in a discipline/subject may be treated as an elective by other discipline/subject and vice versa.

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Table 9: Second Year of MTech (FY MTech VLSI & ES)
Semester IV

Courses				Teaching Scheme Hrs/Week			Examination and Marks (% of Total Curriculum and Marks)				Credit			
							In_Sem Exam (40%)		End_Sem Exam (60%)	Marks				
Course Code	Course Type	Title of Course	Exam Head	Lect	TUT	PR	CCE_1	CCE_2	ESE	Total	TH	TUT	PR	Total
24P1222	INT	Internship$	TW	-	-	$	50	50	150	250	-	-	8	8
24P1223	PCC	MOOC_4	TH	4	-	-	20	20	60	100	4	-	-	4
24P1224	PROJ	Dissertation Stage-II	PROJ	-	-	16	50	50	150	250	-	-	8	8
Total				**-**	**-**	**-**	**240**		**360**	**600**	**4**	**-**	**16**	**20**
Total Hours/ Week				**20**			**600**				**20**			

MOOC_4: NPTEL Courses under SWAYAM for AY 2025-26	
Course Code	**Course Name^**
24P1209-A	Embedded Systems- Design Verification and Test
24P1209-B	Design and Analysis of VLSI Subsystems
24P1209-C	IC Technology
24P1209-D	VLSI Data Conversion Circuits

^Note: Course Names will be declared as per availability of NPTEL courses of 12/16 weeks in that particular year for the semester.

$ Internship:

- Internship corresponding to major courses is to be completed after semester III Examinations and before commencement of semester IV of at least 180 hours/ 6 weeks; and it is to be assessed and evaluated in semester IV.
- It is almost imperative that the commencement of Semester IV needs to be approx. 3 weeks beyond the schedule.

Dr. Jayant J. Chopade
Chairman, BoS & Head , E&TC Engineering

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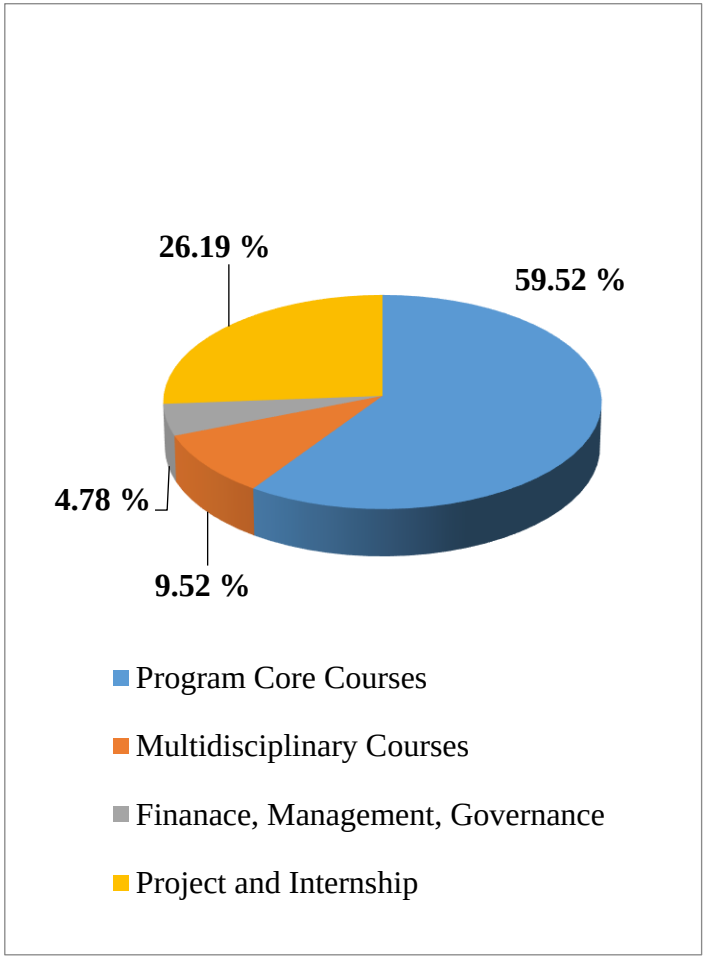
Table 10: Broad Courses' Categories, and Credit Distribution				
Broad Category	**Description**	**Credit**	**Total Credit**	**%**
Program Courses **Total Credit= 50** **59.52%** **(19.00 % in online mode)**	Programme Core Course	30	35	**41.66**
	Programme Core Course Lab	05		
	Programme Elective Course	12	15	**17.85**
	Programme Elective Course Lab	03		
Multidisciplinary Courses **Total Credit = 26** **09.52%**	Multidisciplinary Course	08	08	**09.52**
Project Management, Finance, and Governance **Total Credit =04** **04.78%**	Study of Indian Constitution	01	04	**04.78**
	Project Management and Finance	02		
	Company Law and Governance	01		
Experiential Learning Courses **Total Credit =22** **26.19%**	Dissertation	14	22	**26.19**
	Internship / On Job Training	08		
Total		**84**	**84**	**100**



Matoshri College of Engineering & Research Centre, Nashik
Master of Technology (MTech VLSI & Embedded Systems)

First Year Master of Technology (FY MTech VLSI & Embedded Systems)

24P1201: Physics of VLSI Devices

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Teaching Scheme	Credit	Examination Head: TH		
Lectures: 4 Hrs/week	04	Examination Scheme & Marks		
		ISE	CAT :	20 Marks
			CCE :	20 Marks
		ESE	:	60 Marks
Prerequisite:	Basic Electronics/ Semiconductor Devices			
Companion Course, if any:	Digital design and Embedded system Lab			

Course Objectives:

The course is aimed to:

1. Explicate the fundamentals of intrinsic, extrinsic semiconductors with carrier concentration, modelling and physics of various carrier current transport mechanisms
2. Familiarize detailed physics and modelling of PN Junction, MOS capacitors, and MOSFETs
3. To study the impact of scaling on device performance and reliability
4. Analyze and discuss the short channel effects and the issues of UDSM transistors
5. To explore emerging trends and future directions in VLSI technology
6. To develop skills in designing semiconductor devices, emphasizing the integration of theoretical knowledge with practical applications in real-world problem-solving VLSI technology

Course Outcomes:

On completion of the course, learner will be able to:		BL
CO1:	**Analyze** the principles of semiconductor physics, including carrier concentrations and current flow mechanisms.	4
CO2:	**Evaluate** the electrical characteristics and transient behavior of p-n junctions and document the analysis and design considerations in detailed technical reports.	5
CO3:	**Develop** an understanding of MOS capacitors and MOSFET characteristics, implementing compact models in SPICE for circuit simulation, and solving practical design challenges	6
CO4:	**Analyze** the effects of scaling and short-channel effects on MOSFET performance in modern semiconductor devices, investigating their implications on real-world designs.	4
CO5:	Proactively **investigate** ultra-deep submicron (UDSM) transistor design issues, addressing challenges such as gate leakage, tunneling effects, and their impact on device reliability.	5
CO6:	**Design** and model semiconductor devices considering scaling effects and apply these designs to practical VLSI technology applications, supporting real-world problem-solving and research.	6

Unit-1:	Semiconductor Physics and Carrier Transportation	8 hrs

Energy bands in Intrinsic and Extrinsic semiconductors, Direct and Indirect semiconductors, Carrier Concentrations, Density of states, Fermi-Dirac distribution, Temperature Dependence of Carrier Concentrations, Compensation and Space Charge Neutrality.

Current flow mechanisms: Mobility, Drift current, Diffusion current, Current density equations, Continuity equation.

Unit-II:	**P-N Junctions**	**8 hrs**
Depletion region, junction breakdown, transient behaviour, Thermal equilibrium, Energy band diagrams, Poisson equation, Static current-voltage characteristics of p-n junctions, Depletion layer Capacitance, Heterojunctions.		
Unit-III:	**MOS Capacitor, MOSFETs and Compact Models**	**8 hrs**
MOS Capacitor: Accumulation, Depletion, Week Inversion, Strong Inversion, Channel length modulation, Gate work function, Oxide and Interface charges, Threshold voltage, Current-Voltage Characteristics of MOS MOSFETs: Drain current, Saturation voltage, Sub-threshold conduction, Effect of gate and drain voltage on carrier mobility, Compact models for MOSFET and their implementation in SPICE.		
Unit-IV:	**Scaling and Short Channel Effects**	**7 hrs**
Effect of scaling, Channel length modulation, Punch-through, Hot carrier degradation, MOSFET breakdown, Drain-induced barrier lowering.		
Unit-V:	**UDSM Transistor Design Issues**	**7 hrs**
Effect of tox, Effect of high-k and low-k dielectrics on the Gate leakage, Source and Drain leakage, Tunnelling effects, Different gate structures in UDSM, Impact and reliability challenges in UDSM.		

Text Books:

1]. **"Solid State Electronic Devices",** Ben G. Streetman and S. Banerjee, Pearson Education, U.S, Seventh Edition, 2014.
2]. **"Physics of Semiconductor Devices",** J.P. Colinge and C. A. Colinge, Kluwer Academic Publishers, US, 2017.
3]. **"Physics of Semiconductor Devices",** S.M.SZE, Kwok K. Ng, John Wiley & Sons, third edition, 2006.

Reference Books:

1]. **"Operation and Modelling of the MOS Transistor",** Y.P. Tsividis and Colin McAndrew, Oxford University Press, US, Third Edition, 2011.
2]. **"Fundamental of Semiconductor Devices",** M K Achutan and K N Bhatt, McGraw Hill Education, US, 2017.
3]. **"Fundamentals of Semiconductors",** Peter Y. Yu, Manuel Cardona, Fourth edition, Springer, 2010.

The CO-PO Mapping Matrix:

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**
CO1	2		2	1			2	1
CO2	2	3					1	
CO3	2		3			2	2	3
CO4	1		2	2			3	2
CO5	2			3			3	3
CO6	3		3			2	3	3

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First Year Master of Technology (FY MTech VLSI & Embedded Systems)

24P1202: MOOC_1

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Teaching Scheme	Credit	Examination Head: TH		
Lectures: 4 Hrs/week	4	Examination Scheme & Marks		
		ISE	CAT :	20 Marks
			CCE :	20 Marks
		ESE	:	60 Marks

Guidelines

This course aims to create an opportunity for students to acquire the necessary skill set for employability through massive online courses where the rare expertise of world famous experts from academics and industry are available.
MOOCs (**Massive Open Online Courses**) provide an affordable and flexible way to learn new skills. MOOCs are courses delivered online and accessible to all for free. Massive because enrolments are unlimited and can run into hundreds of thousands. Open because anyone can enroll — that is, there is no admission process. Online because they are delivered via the internet. Course because their goal is to teach aspecific subject. MOOCs typically comprise video lessons, readings, assessments, and discussion forums.

Learner has to select one of the following courses and successfully complete the same:

Course Code	Course Name (Udemy) for AY 2024-25
24P1202-A	**CMOS Analog Circuit Design** https://www.udemy.com/course/analog_ic_design_overview/
24P1202-B	**Introduction to VHDL for FPGA and ASIC design** https://www.udemy.com/course/introduction-to-vhdl-for-fpga-and-asic-design/
24P1202-C	**Analog Circuit Design - An Intuitive Approach** https://www.udemy.com/course/analog-circuit-design-intuitive-approach-to-design
24P1202-D	**VLSI Design** https://www.udemy.com/course/vlsi-design-mask/

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24P1203: Research Methodology

Teaching Scheme	Credit	Examination Head: TH		
Lectures: 2 Hrs/week	2	Examination Scheme & Marks		
		ISE	CAT :	20 Marks
			CCE :	20 Marks
		ESE	:	60 Marks
Companion Course, if any:	Digital design and Embedded system Lab (24P1206)			

Course Objectives:

- To understand basic concepts of research and its methodologies
- To learn the methodology to conduct the Literature Survey
- To acquaint with the tools, techniques, and processes for statistical analysis
- To effectively use and compare optimization techniques for solving problems involving single and multi-parameter cost functions
- To understanding sampling theory and its application in research

Course Outcomes:

On completion of the course, learner will be able to:		BL
CO1:	**Identify** fundamental concepts, purposes, processes, and motivations of research, encompassing various paradigms, types, and scientific postulates.	1
CO2:	**Conduct** a literature survey, define a clear research statement, develop a comprehensive research plan, identify diverse research tools, and present the report.	5
CO3:	**Conduct** comprehensive statistical analyses, including error and uncertainty assessments, and perform hypothesis testing on research data.	4
CO4:	**Apply** various optimization techniques to solve complex research problems involving single and multi-parameter cost functions and, present the results and methodologies in a comprehensive technical report.	3
CO5:	**Apply** sampling theory and estimation techniques to determine sample size for estimating population parameters in research by presenting the findings.	3
CO6:	**Develop** the skills to conduct comprehensive research, encompassing the definition of research statements, literature surveys, and the application of statistical analyses, optimization techniques, and sampling methods. Use these skills to provide innovative solutions for complex, real-life problems, and present your findings in a substantial technical report.	5

Course Contents

Unit-I:	Introduction	07 Hours

Evolution of Research Methodology: Meaning, nature, scope, and significance of research; Research paradigm; The purpose and Products of Research; Reasons for doing research, Objectives of research, Motivation for research; Postulates underlying scientific investigations; Types of research; Research process and work flow.

Engineering Research-Why? Research Questions, Engineering Ethics, conclusive proof-what constitutes A research project-Why take on?

Case Studies (if any)	Code of Ethics, IEEE Code of Ethics, ACM Software Engineering Code of Ethics and Professional Practice, Code of Ethics especially covering Engineering discipline, various aspects- environment, sustainable outcomes, employer, general public, & Nation, Engineering Disasters

Unit-II:	Literature Search and Review, developing Research Plan	07 Hours

Archival Literature, why should engineers be ethical? Types of publications- Journal papers, conference papers, books, standards, patents, theses, trade magazine, newspaper article, infomercials, advertisement, Wikipedia & websites, Measures of research impact, Literature review, publication cost.

Developing Research Plan: Research Proposals, finding suitable research questions, The elements of research proposals-title, details, budget, Design for outcomes-1D data, 2D data, 3D data, N-D data, The research tools- Experimental measurements, numerical modeling, theoretical derivations & Calculations, curve matching.		
Case Studies (if any)	Engineering dictionary, Shodhganga, The Library of Congress, Research gate, Google Scholar, Bibliometrics, Citations, Impact Factor, h-index, I-index, plagiarism, copyright infringement. Collect data for overbooking decision for demand and revenue management of flights	
Unit-III:	**Statistical Analysis**	**07 Hours**
Statistical Analysis: Introduction, Sources of error and uncertainty, One-Dimensional Statistics: combining errors and uncertainties, t-test, ANOVA statistics, example, Two-Dimensional Statistics: example, Multi-Dimensional Statistics: partial correlation coefficients, example, Null hypothesis testing.		
Case Studies (if any)	GNU PSPP Tool, SOFA, NOST-Dataplot	
Unit-IV:	**Optimization Techniques**	**07 Hours**
Optimization Techniques: Introduction, Two-parameter optimization methods: sequential uniform sampling, Monte Carlo optimization, Simplex Optimization method, Gradient Optimization method, multi-parameter optimization methods, The cost function.		
Case Studies (if any)	Google Optimization Tools, OpenMDAO	
Unit-V:	**Data Sampling**	**07 Hours**
Sampling Fundamentals: Need for Sampling, Some Fundamental Definitions, Important Sampling Distributions, Central Limit Theorem, Sampling Theory, Sandler's A-test, Concept of Standard Error, Estimation, Estimating the Population Mean (μ), Estimating Population Proportion, Sample Size and its Determination.		
Case Studies (if any)	Determination of Sample Size through the Approach Based on Precision Rate and Confidence Level	

Text Books:

1]. David V Thiel, "Research Methods- for Engineers", Cambridge University Press, ISBN:978-1-107-61019-4

2]. Kothari C.R., "Research Methodology. New Age International, 2004, 2nd Ed; ISBN:13: 978-81-224-1522-3.

Reference Books:

1]. Caroline Whitbeck, "Ethics in Engineering Practice and Research", 2nd Ed., Cambridge University Press; ISBN :978-1-107-66847-8

2]. Gordana DODIG-CRNKOVIC, "Scientific Methods in Computer Science", Department of Computer Science Malardalen University, Vasteas, Sweden; ISBN: 91-26-97860-1

E-books:

1]. Research Methodology- https://www.drnishikantjha.com/papersCollection/Research%20Methodology%20.pdf

2]. Research Methodology Tools and Techniques- https://www.euacademic.org/BookUpload/9.pdf

MOOC Courses

- Introduction to Research- https://onlinecourses.nptel.ac.in/noc23_ge36/preview
- Research Methodology- https://onlinecourses.nptel.ac.in/noc22_ge08/preview
- Introduction to Research- https://nptel.ac.in/courses/121106007

The CO-PO Mapping Matrix:

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2
CO1	2		2	2			1	1
CO2	3	3		2			2	2
CO3	3		2				1	3
CO4	3	3	2	3			3	3
CO5	2		3	2			2	3
CO6	3	3	3	3			3	3

Matoshri College of Engineering & Research Centre, Nashik
Master of Technology (MTech VLSI & Embedded Systems)

First Year Master of Technology (FY MTech VLSI & Embedded Systems)

24P1204: Embedded System Design

Teaching Scheme	Credit	Examination Head: TH		
Lectures: 4 Hrs/week	4	Examination Scheme & Marks		
		ISE	CAT :	20 Marks
			CCE :	20 Marks
		ESE	:	60 Marks
Prerequisite:	Digital system and Microcontrollers			
Companion Course, if any:	Digital design and Embedded System lab			

Course Objectives:

- Introduce meaning of Embedded system
- Study ARM CORTEX Processor based Embedded System design for real-world applications
- Demonstrate the knowledge of interfacing with STM 32
- Explore Linux operating system and device driver.
- Enable the students to Understand embedded system development process and tools.
- To provide hands-on experience in real-time embedded systems applications using advanced processors and tools.

Course Outcomes:

On completion of the course, learner will be able to:		BL
CO1:	**Analyze** the definition and core characteristics of embedded systems to identify and classify real-world applications.	4
CO2:	**Design** embedded systems using ARM Cortex processors and document the design process, analysis, and results through comprehensive technical reports and presentations.	5
CO3:	**Develop** and **apply** interfacing techniques for STM32 microcontrollers in embedded applications, demonstrating efficient hardware integration.	6
CO4:	**Utilize** and configure the Linux operating system and device drivers for embedded systems, assessing their role in system performance.	5
CO5:	Independently **design** and **implement** innovative real-time embedded systems using modern processors and tools, focusing on research-driven practical applications and problem-solving.	6
CO6:	**Develop** and implement innovative practical real-time embedded systems using modern processors, tools, and techniques.	6

Unit-1:	Introduction to Embedded system	7 hrs

Definition and characteristics of embedded systems, Design metrics, Concept of Embedded system design: Design challenge, Processor technology, IC technology, Design technology Development platform - Arduino, Raspberry-PI, MSP430 (introduce IDE and board Details)

Unit-II:	ARM CORTEX Processors	8 hrs

ARM CORTEX series features, CORTEX A, R, M processors series comparison, Survey of CORTEX based controllers from various manufacturers, ARM-M3 Based Microcontroller LPC1768: Features, Architecture (Block Diagram & It's Description), System Control, Clock & Power Control, Pin Connect Block. CMSIS Standard, Bus Protocols like CAN, USB.

Unit-III:	Embedded System Design with STM32	8 hrs

Architectural review of STM32F4XX MCU**:** Pin diagram, CPU, Memory, GPIO, Clock and Timer module, ADC-DAC module, Study of STM32F4 Development board, Software development tool SM32CubeIDE, Debugging with STM32CubeIDE, IDEs for STM32; Sample codes in C for

Toggling an LED, reading a switch and displaying it on an LED, display a message on the LCD using 8-bitmode and delay.

Unit-IV:	**Embedded Linux and Device Driver**	**8 hrs**

Introduction, Embedded Linux Today, Open Source and the GPL, Kernel Versions, Kernel Source Repositories, using Git to Download a Kernel, Linux Kernel Construction, Kernel Build System, Kernel Configuration, BIOS versus boot-loader, Role of a Bootloader, A Universal Bootloader: Das U-Boot, Device Driver Basics, Linux File System Concepts.

Unit-V:	**Embedded System Design Case Studies**	**7 hrs**

Embedded software development process and tools – introduction, host and target machine, linking and locating software, Getting Embedded software to target system, Issues in hardware and software design and co-design, Design Case Studies: Automated Meter Reading Systems (AMR), Digital Camera.

Text Books:

1]. **"Embedded system Design: A Unified Hardware/Software Introduction"**, Frank Vahid, Tony D. Givargis, New Delhi: Wily India Pvt. Ltd.

2]. "**ARM System Developer's Guide – Designing and Optimizing System Software**", Andrew Sloss, Dominic Symes, Chris Wright, Elsevier, 1st Edition

3]. "**Mastering STM32",** Carmine Noviello, Lean Publisher,2nd Edition,2018.

4]. **"Embedded Linux Primer:** A Practical, Real-World Approach**",** Christopher Hallinan,Prentice Hall, Second Edition,2011.

5]. **"Embedded Systems: Architecture, Programming and Design**",Raj Kamal, 2nd ed. New Delhi: Tata McGraw Hill Education India Private Limited, 2008.

Reference Books:

1]. "**An Embedded Software Primer",**David E. Simon, Pearson Education,2001.

2]. "**STM32 Arm Programming for Embedded Systems: Using C Language with STM32**", Shujen Chen, Muhammad Ali Mazidi, Eshragh Ghaemi, Nucleo, Micro DigitalEd., Illustrated Edition,2018

3]. **"Embedded Systems Architecture"**A Comprehensive Guide for Engineers and Programmers**",**Tammy Noergaard, Elsevier,2005.

4]. "**Introduction to Embedded Systems",** Shibu K V, TMH,2nd Edition,2009.

MOOC / NPTEL Courses:

1. NPTEL Course on "**Embedded System Design with ARM**", by Prof. Indranil Sengupta,and Prof. Kamalika Datta, IIT Kharagpur
Link of the Course: https://nptel.ac.in/courses/106105193

2.NPTEL Course on, **"Introduction to Embedded System Design"**, by Prof. D.V.Gadre, Prof.B.N. Subudhi IIT Jammu
Link of the course: https://nptel.ac.in/courses/108102169

The CO-PO Mapping Matrix:

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2
CO1	2		2				2	1
CO2	2	3	2			2	3	2
CO3	3		2			3	2	3
CO4	2		3	2		2	2	3
CO5	3		3	3	3	3	3	3
CO6	3	2	3	3	3	3	3	3

Matoshri College of Engineering & Research Centre, Nashik
Master of Technology (MTech VLSI & Embedded Systems)

First Year Master of Technology (FY MTech VLSI & Embedded Systems)

Elective-I

24P1205-A: Micro Electromechanical Systems

Teaching Scheme	Credit	Examination Head: TH		
		Examination Scheme & Marks		
Lectures: 4 Hrs/week	04	ISE	CAT :	20 Marks
			CCE :	20 Marks
		ESE	:	60 Marks
Prerequisite:	--			
Companion Course, if any:	Elective Course-I Lab			

Course Objectives:

- To provide a comprehensive understanding of MEMS technology, including its principles, fabrication techniques, and applications
- To familiarize students with various MEMS devices and their real-world applications.
- To develop the ability to design and simulate MEMS devices using modern tools and techniques
- To explore advanced topics and emerging trends in MEMS and their potential impact
- To prepare students for research and development in the field of MEMS technology.
- To enable students to apply MEMS technology principles in interdisciplinary fields and foster innovation in microsystems design.

Course Outcomes:

On completion of the course, learner will be able to:		BL
CO1:	Independently **analyze** the evolution and applications of MEMS across various industries and assess the impact of microfabrication processes and materials on MEMS technology.	**4**
CO2:	**Evaluate** MEMS fabrication techniques such as bulk micromachining, surface micromachining, and high-aspect-ratio micromachining, and present a detailed technical report documenting the analysis and applications of these techniques.	**5**
CO3:	**Develop** models of MEMS sensors and actuators, exploring their use in real-world applications such as RF MEMS and optical MEMS, with an emphasis on case studies while conducting independent research to support findings.	**6**
CO4:	**Apply** principles of MEMS design and perform simulation using Finite Element Analysis (FEA) tools, considering mechanical, electrical, and thermal factors in MEMS development, and document the design process effectively.	**5**
CO5:	**Investigate** advanced topics and emerging trends in MEMS such as NEMS, BioMEMS, energy harvesting, and MEMS integration with CMOS technology, identifying future trends and innovations through independent research efforts.	**5**
CO6:	Independently **design**, **develop**, and **evaluate** MEMS-based systems, demonstrating research-driven approaches to solving complex real-world problems in engineering.	**6**

Unit-1:	**Introduction to MEMS**	**7 hrs**

Definition and evolution of MEMS, Applications of MEMS: Automotive, biomedical, telecommunications, and consumer electronics.
Basic concepts of microfabrication: Photolithography, etching, and deposition, Materials for MEMS: Silicon, polymers, metals, and ceramics, Overview of MEMS markets and trends

Unit-II:	**MEMS Fabrication Techniques**	**8 hrs**
Bulk micromachining: Isotropic and anisotropic etching, Surface micromachining: Sacrificial layer processes, thin-film deposition, High-aspect-ratio micromachining: LIGA, DRIE, Bonding techniques: Wafer bonding, anodic bonding, and fusion bonding, Packaging of MEMS devices: Challenges and solutions		
Unit-III:	**Models MEMS Devices and Applications**	**8 hrs**
Sensors: Pressure sensors, accelerometers, gyroscopes, and biosensors; Actuators: Electrostatic, thermal, piezoelectric, and magnetic actuators; RF MEMS: Switches, resonators, and filters; Optical MEMS: Micro-mirrors, optical switches, and MOEMS devices; Case studies of MEMS devices in real-world applications		
Unit-IV:	**MEMS Design and Simulation**	**8 hrs**
Principles of MEMS design: Mechanical, electrical, and thermal considerations; Finite Element Analysis (FEA) for MEMS: Modelling and simulation tools; Multiphysics simulation: Coupled-field analysis; Design for manufacturability and reliability; Case studies: Design and simulation of MEMS devices		
Unit-V:	**Advanced Topics and Emerging Trends in MEMS**	**8 hrs**
NEMS (Nanoelectromechanical Systems): Concepts and applications; BioMEMS: Lab-on-a-chip, microfluidics, and medical devices; Energy harvesting using MEMS; Integration of MEMS with CMOS technology; Future trends in MEMS: Flexible electronics, wearable MEMS, and IoT applications		

Text Books:

1]. **"MEMS Mechanical Sensors**", Stephen Beeby, Graham Ensell, Michael Kraft and Neil White, Artech House Publications
2]. **"Microsystem Design",** Stephen D. Senturia, Kluwer Academic Publishers
3]. **"Microsensors, MEMS and Smart Devices: Technology, Applications and Devices",** Julian W. Gardner, Vijay K. Varadan, Julian Publications

Reference Books:

1]. **"The MEMS Handbook",** Mohamed Gad-el-Hak, Taylor & Francis Group
2]. **"Handbook of Silicon Based MEMS Materials and Technologies",** Markku Tilli, Teruaki Motooka, Veli-Matti Airaksinen, Elsevier Inc.
3]. **"MEMS: A Practical Guide to Design, Analysis, and Applications",** Jan G. Korvink and Oliver Paul
4]. **"RF MEMS and Their Applications",** Vijay K. Varadan, K. J. Vinoy, and K. A. Jose, John Wiley & Sons Ltd

The CO-PO Mapping Matrix:

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2
CO1	2		3	2			2	2
CO2	3	3	2			2	2	3
CO3	3		3	2		2	3	3
CO4	3		3	2		3	3	3
CO5	3		3	3	3	2	3	3
CO6	3	3	3	3	3	3	3	3

Matoshri College of Engineering & Research Centre, Nashik
Master of Technology (MTech VLSI & Embedded Systems)

First Year Master of Technology (FY MTech VLSI & Embedded Systems)

Elective-I

24P1205-B: VLSI Digital Signal Processing

Teaching Scheme	Credit	Examination Head: TH		
		Examination Scheme & Marks		
Lectures: 4 Hrs/week	04	ISE	CAT :	20 Marks
			CCE :	20 Marks
		ESE	:	60 Marks
Prerequisite:	Digital Signal Processing, VLSI			
Companion Course, if any:	Elective course-1 lab			

Course Objectives:

- To provide a comprehensive understanding of VLSI technology and its application in DSP.
- To familiarize students with various VLSI architectures for implementing DSP algorithms.
- To explore low-power and high-performance design techniques for DSP systems.
- To develop proficiency in implementing DSP algorithms on VLSI platforms.
- To introduce advanced topics and emerging trends in VLSI DSP design.
- To equip students with the ability to integrate VLSI design techniques with DSP applications for real-world problem-solving.

Course Outcomes:

On completion of the course, learner will be able to:		BL
CO1:	**Analyze** the fundamentals of Digital Signal Processing (DSP) and the significance of VLSI technology in DSP system design, including low-power and high-performance design considerations.	4
CO2:	Document and present a comprehensive evaluation of various VLSI architectures for DSP, focusing on data flow, control flow graphs, pipelining, and parallel processing techniques, while assessing their impact on performance.	5
CO3:	Independently **develop** low-power and high-performance design methodologies for DSP systems, applying techniques such as clock gating and voltage scaling, while analyzing case studies of real-world applications.	6
CO4:	Conduct **research** on the implementation of DSP algorithms on VLSI systems, including FIR and IIR filters, FFT, and DCT, demonstrating practical skills through case studies of adaptive filters and their VLSI implementations.	6
CO5:	**Investigate** advances in VLSI DSP design, including wireless communication systems, reconfigurable DSP systems, and emerging trends such as neuromorphic computing and deep learning accelerators, focusing on problem-solving.	5
CO6:	Independently **design**, **develop**, and **evaluate** innovative VLSI-based DSP systems, demonstrating a comprehensive understanding of DSP algorithms and their practical applications in modern technology.	6

Unit-1:	**Introduction to VLSI Digital Signal Processing**	**8 hrs**

Basics of Digital Signal Processing (DSP), Overview of VLSI technology for DSP, DSP system design: Architectures and methodologies Importance of low-power and high-performance DSP design, Review of signal processing algorithms: FIR, IIR filters, FFT, and DCT

Unit-II:	**VLSI Architectures for DSP**	**8 hrs**

Data flow and control flow graphs, Pipelining and parallel processing techniques, Systolic array architectures, Retiming and unfolding, Folding transformation		
Unit-III:	**Low-Power and High-Performance DSP Design**	**8 hrs**
Power consumption in DSP systems, Power reduction techniques: Clock gating, power gating, and voltage scaling, Low-power design methodologies for DSP, High-performance design techniques: Pipelining, parallelism, and hardware accelerators, Case studies: Low-power and high-performance DSP applications		
Unit-IV:	**Implementation of DSP Algorithms on VLSI**	**7 hrs**
Implementation of FIR and IIR filters on VLSI, Fast Fourier Transform (FFT) and its VLSI implementation, Discrete Cosine Transform (DCT) and its VLSI implementation, Adaptive filters: LMS and RLS algorithms, Case studies: Practical VLSI implementation of DSP algorithms		
Unit-V:	**Advances in VLSI DSP**	**7 hrs**
VLSI design for wireless communication systems Design of reconfigurable DSP systems, Emerging trends in VLSI DSP: Neuromorphic computing, deep learning accelerators, ASIC and FPGA-based DSP design, Future directions and challenges in VLSI DSP		
Text Books:		
1]. **"VLSI Digital Signal Processing Systems: Design and Implementation",** Keshab K. Parhi, John Wiley, 1999 2]. **"Digital Integrated Circuits: A Design Perspective",** Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, Prentice Hall ,2nd Edition 3]. **"Digital Signal Processing: A Practical Approach",** Emmanuel C. Ifeachor and Barrie W. Jervis, Prentice Hall, 2nd Edition,2002.		
Reference Books:		
1]. **"Digital Signal Processing: Principles, Algorithms, and Applications",** John G. Proakis and Dimitris G. Manolakis, Prentice Hall, 2nd Edition,1996. 2]. **"Design of High-Performance Microprocessor Circuits",** Anantha Chandrakasan, William J. Bowhill, and Frank Fox, Willy, IEEE press,2001. 3]. **"CMOS VLSI Design: A Systems Perspective",** Neil H.E. Weste, David Money Harris, Addison-Wesley, 4th Edition, 2011.		

The CO-PO Mapping Matrix:

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2
CO1	2		3			2	3	2
CO2	2	3	3			2	2	3
CO3	3		3			3	3	3
CO4	3		3	2		2	3	3
CO5	3		3	3	3		3	3
CO6	3	2	3	3	3	3	3	3

Matoshri College of Engineering & Research Centre, Nashik
Master of Technology (MTech VLSI & Embedded Systems)

First Year Master of Technology (FY MTech VLSI & Embedded Systems)

Elective-I

24P1205-C: Low Power IC Design

Home

Teaching Scheme	Credit	Examination Head: TH		
		Examination Scheme & Marks		
Lectures: 4 Hrs/week	4	ISE	CAT :	20 Marks
			CCE :	20 Marks
		ESE	:	60 Marks
Prerequisite:	--			
Companion Course, if any:	Elective Course-I Lab			

Course Objectives:

- To provide a comprehensive understanding of the importance and challenges of low power IC design.
- To familiarize students with various techniques to reduce power consumption at different levels of design abstraction.
- To develop proficiency in designing low power circuits and systems using state-of-the-art tools and methodologies.
- To explore advanced topics and emerging trends in low power IC design.
- To prepare students for research and development in the field of low power electronics.
- To enable students to integrate low power design techniques into the overall IC design process, ensuring energy efficiency across different applications.

Course Outcomes:

On completion of the course, learner will be able to:		BL
CO1:	**Analyze** the importance of low power design in modern electronics, identifying power dissipation mechanisms and estimation techniques used in digital circuits.	4
CO2:	**Document** and present the evaluation of circuit-level low power design techniques, such as dynamic voltage and frequency scaling, to optimize power consumption in digital systems.	5
CO3:	**Develop** architectural-level low power design strategies, including clock gating and energy-efficient memory design, to enhance overall system performance.	6
CO4:	**Conduct** independent research on and implement system-level power management techniques, including hardware-software co-design and power-aware communication protocols, in real-world applications.	6
CO5:	**Investigate** emerging low power technologies and their applications in various domains, focusing on design automation tools and future trends in low power IC design, while presenting findings in a comprehensive technical report.	5
CO6:	Independently **design** and **evaluate** innovative low power integrated circuits, demonstrating a comprehensive understanding of low power design techniques and their practical applications	6

Unit-1:	Introduction to Low Power Design	8 hrs

Importance of low power design in modern electronics; Sources of power dissipation in digital circuits; Power dissipation mechanisms: Dynamic, static, and short-circuit power; Power estimation techniques: Gate-level, RTL-level, and system-level Metrics for power efficiency: Energy per operation, power-delay product

Unit-II:	**Low Power Design Techniques at the Circuit Level**	**8 hrs**
Transistor sizing, optimization for low power, Dynamic voltage and frequency scaling, Power gating and multi-threshold CMOS, Adaptive body biasing, Leakage power reduction techniques: Sleep transistors, stack forcing, and reverse body biasing		
Unit-III:	**Low Power Design Techniques at the Architectural Level**	**8 hrs**
Clock gating and power gating Operand isolation and data path optimization Low power memory design: SRAM, DRAM, and non-volatile memories Energy-efficient arithmetic units: Adders, multipliers, and dividers Power-aware design of FPGAs and ASICs		
Unit-IV:	**Low Power Design Techniques at the System Level**	**7 hrs**
System-level power management: Hardware-software co-design, Power-aware communication protocols and interfaces, Low power techniques for wireless systems and IoT devices, Power management in mobile and wearable devices Case studies: Low power design in real-world applications		
Unit-V:	**Advances in Low Power IC Design**	**7 hrs**
Emerging low power technologies: F in FETs, TFETs, and NEM relays, Ultra-low power circuits for biomedical and implantable devices, Power-efficient design for machine learning accelerators Design automation tools for low power IC design Future trends and challenges in low power IC design		

Text Books:

1]. **"Low-Power Digital VLSI Design: Circuits and Systems**", Abdellatif Bellaouar and Mohamed I. Elmasry, Springer Science + Business Media, 1995.

2]. **"Low-Power High-Resolution Analog to Digital Converters:** Design, Test and Calibration**",** Amir Zjajo, Springer Science + Business Media, 2011.

3]. **"Low-Power CMOS Circuits:** Technology, Logic Design and CAD Tools **",** Christian Piguet, CRC Press,2006.

Reference Books:

1]. **"Low-Power VLSI Circuits and Systems",** Ajit Pal, Springer,2015.

2]. **"Low Power VLSI Design" ,** Angsuman Sarkar, Swapnadip De, Manash Chanda, Chandan Kumar Sarkar, DE Gruyter, 2016.

3]. **"Low-Power Design Techniques and CAD Tools for Analog and RF Integrated Circuits",** Piet Wambacq, Georges Gielen, Kluwer Academic Publishers, 2001.

The CO-PO Mapping Matrix:

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2
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CO2	3	3	2			2	2	3
CO3	3		3			3	3	3
CO4	3		3	3	3	2	3	3
CO5	3		3	3	2		3	3
CO6	3	3	3	3	3	3	3	3

Matoshri College of Engineering & Research Centre, Nashik
Master of Technology (MTech VLSI & Embedded Systems)

First Year Master of Technology (FY MTech VLSI & Embedded Systems)

Elective-I

24P1205-D: System Design with FPGA

Home

Teaching Scheme	Credit	Examination Head: TH		
Lectures: 4 Hrs/week	4	Examination Scheme & Marks		
		ISE	CAT :	20 Marks
			CCE :	20 Marks
		ESE	ESE :	60 Marks
Prerequisite:	Digital Circuits/VLSI Design			
Companion Course, if any:	Elective Course-I Lab			

Course Objectives:

- To provide a comprehensive understanding of FPGA technology and its applications in system design.
- To familiarize students with FPGA design tools, methodologies, and design flows.
- To develop proficiency in implementing complex algorithms and systems on FPGAs.
- To explore advanced FPGA architectures and design techniques.
- To prepare students for research and development in FPGA-based system design.
- To equip students with the ability to optimize FPGA-based designs for specific applications, ensuring efficiency in performance, area, and power.

Course Outcomes:

On completion of the course, learner will be able to:		**BL**
CO1:	**Analyze** the architecture of Field-Programmable Gate Arrays (FPGAs), including CLBs, IOBs, interconnects, and routing resources, and compare FPGA families from vendors such as Xilinx, Intel, and Lattice, assessing their suitability for specific design requirements.	**4**
CO2:	**Design** and implement FPGA-based systems using HDLs and modern design tools, presenting the complete design process through technical reports that document the synthesis, implementation, and verification stages.	**6**
CO3:	**Analyse** FPGA designs for performance, area, and power.	**4**
CO4:	**Integrate** FPGAs into embedded systems and high-performance computing applications.	**5**
CO5:	**Conduct** independent research on advanced topics and emerging trends in FPGA technology, including machine learning accelerators and reconfigurable computing, to contribute to innovative solutions in modern applications.	**5**
CO6:	Independently **investigate** and apply advanced techniques such as pipelining, parallelism, and low-power methodologies to optimize FPGA-based designs, addressing practical challenges in performance, area, and power efficiency through innovative solutions.	**5**

Unit-1:	**Introduction to FPGA Technology**	**8 hrs**

Overview of Field-Programmable Gate Arrays (FPGAs), FPGA architecture: CLBs, IOBs, interconnects, and routing resources, FPGA families and vendors: Xilinx, Intel (Altera), Lattice, and others, FPGA design flow: Design entry, synthesis, implementation, and verification Introduction to HDLs: Verilog and VHDL for FPGA design.

Unit-II:	**FPGA Design Tools and Methodologies**	**8 hrs**

FPGA design software: Xilinx Vivado, Intel Quartus Prime, and others, Design constraints and timing analysis, IP cores and FPGA design reuse, Simulation and verification of FPGA designs, Design for testability (DFT) techniques for FPGAs		
Unit-III:	**Advanced FPGA Architectures and Design Techniques**	**8 hrs**
High-level synthesis (HLS) for FPGA design, Design optimization techniques: Pipelining, parallelism, and resource sharing, Implementing complex algorithms on FPGAs: FFT, image processing, and digital signal processing, FPGA-based embedded systems: ARM-based SoCs and MicroBlaze/Nios II processors, Case studies: Real-world applications of advanced FPGA designs		
Unit-IV:	**FPGA-Based System Design**	**7 hrs**
FPGA-based prototyping and emulation, System integration using FPGAs: Interfacing with peripherals and sensors, Communication protocols on FPGAs: Ethernet, PCIe, USB, and CAN Real-time operating systems (RTOS) on FPGAs, FPGA-based co-processing and acceleration techniques		
Unit-V:	**Advanced Topics in FPGA Design**	**7 hrs**
Reconfigurable computing with FPGAs, FPGA-based machine learning accelerators, Low-power design techniques for FPGAs, Security considerations in FPGA designs, Emerging trends and future directions in FPGA technology.		

Text Books:

1. "FPGA-Based System Design", Wayne Wolf
2. "Digital Design and Computer Architecture", David Harris and Sarah Harris
3. "FPGA Prototyping by VHDL Examples: Xilinx Spartan-6 Version", Pong P. Chu
4. "Digital Design: Principles and Practices", John F. Wakerly
5. "FPGA-Based System Design", Madhavi Agrawal

Reference Books:

1. "FPGA-Based Digital Signal Processing", Roger Woods, John McAllister, and Gaye Lightbody
2. "FPGA Prototyping for SoC Verification", Andrew G. Schmidt, Jingcao Hu, and Greg Tumbush
3. "Digital Design and Computer Architecture: ARM Edition", Sarah Harris and David Harris
4. "FPGA Implementation of Artificial Neural Networks", Tarek S. Abdelrahman
5. "Programming FPGAs: Getting Started with Verilog", Simon Monk

The CO-PO Mapping Matrix:

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2
CO1	2		3			2	3	3
CO2	2	3	2			2	3	3
CO3	3		3			3	3	3
CO4	3		3	3	3	2	3	3
CO5	3		3	3	2		3	3
CO6	3	2	3	3	3	3	3	3

Matoshri College of Engineering & Research Centre, Nashik
Master of Technology (MTech VLSI & Embedded Systems)

First Year Master of Technology (FY MTech VLSI & Embedded Systems)

24P1206: Digital design and Embedded system Lab

Home

Teaching Scheme	Credit	Examination Head: PR
Practical: 4 Hrs/week	**2**	**Examination Scheme & Marks** **ISE : 20 Marks** **ESE: 30 Marks**

Course Objectives:

- Understand and analyze the fundamental principles of semiconductor physics, including carrier concentration and current flow mechanisms, and apply mathematical models and simulations to evaluate these properties in intrinsic and extrinsic semiconductors
- Develop critical research skills by analyzing academic literature in the field of engineering, evaluating experimental verification methods, and assessing the accuracy and validity of research findings
- Perform statistical and citation analysis of published research articles, identifying trends in citations and key performance metrics, and apply these insights to evaluate the impact and relevance of research work
- Master embedded system design by working with ARM Cortex-M3 and STM32 microcontrollers, implementing and simulating hardware-software integration for various embedded applications
- Design and implement real-time embedded systems for practical applications, such as sensor-based systems, clap detection, and automated meter reading, integrating sensors and communication protocols effectively
- Apply advanced programming techniques and use embedded development tools to build and debug software for controlling embedded hardware, demonstrating problem-solving skills in real-world scenarios

Course Outcomes:

On completion of the course, learner will be able to:		**BL**
CO1:	**Analyze** and simulate carrier concentration variations in intrinsic and extrinsic semiconductors using Fermi-Dirac distribution and MATLAB.	**4**
CO2:	**Develop** MATLAB models to simulate current flow mechanisms in semiconductors and evaluate drift and diffusion currents based on electric field and concentration gradients.	**6**
CO3:	Critically **evaluate** research papers in the engineering discipline, analyzing the verification methods and assessing the validity of the research conclusions.	**5**
CO4:	**Conduct** a thorough statistical and numerical analysis of published journal articles in the field, identifying key metrics and comparing citation trends.	**5**
CO5:	**Design** and **implement** embedded system applications using ARM Cortex-M3 and STM32 microcontrollers, demonstrating the ability to develop software for hardware control.	**6**
CO6:	Independently **design** and evaluate real-time embedded systems for practical applications like clap detection and AMR systems, showcasing the integration of sensors and communication protocols.	**6**

Guidelines for Instructor's Manual

The instructor's manual is to be developed as a hands-on resource and reference. The instructor's manual need to include prologue (about University/program/ institute/ department/foreword/ preface etc.), copy of curriculum, conduction & Assessment guidelines, topics under consideration-concept, objectives, outcomes, set of typical applications/assignments/ guidelines, and references.

Guidelines for Student's Lab Journal

The laboratory assignments are to be submitted by student in the form of journal. Journal consists of prologue, Certificate, table of contents, and handwritten write-up of each assignment (Title, Objectives, Problem Statement, Outcomes, software & Hardware requirements, Date of

Completion, Assessment grade/marks and assessor's sign, Theory-Concept in brief, features of tool/framework/language used, Design, test cases, conclusion. Program codes with sample output of all performed assignments are to be submitted as softcopy.
As a conscious effort and little contribution towards Green IT and environment awareness, attaching printed papers as part of write-ups and program listing to journal may be avoided. Use of DVD containing students programs maintained by lab In-charge is highly encouraged. For reference one or two journals may be maintained with program prints at Laboratory.

Guidelines for Lab /TW Assessment

Continuous assessment of laboratory work is done based on overall performance and lab assignments performance of student. Each lab assignment assessment will assign grade/marks based on parameters with appropriate weightage. Suggested parameters for overall assessment as well as each lab assignment assessment include- timely completion, performance, innovation, efficient codes, punctuality and neatness.

Guidelines for Laboratory Conduction

List of laboratory assignments is provided below for reference. The instructor is expected to frame the assignments by understanding the prerequisites, technological aspects, utility and recent trends related to the topic. The assignment framing policy need to address the average students and inclusive of an element to attract and promote the intelligent students. The instructor may set multiple sets of assignments and distribute among batches of students. It is appreciated if the assignments are based on real world problems/applications. Encourage students for appropriate use of coding style, proper indentation and comments. **Use of open-source software and recent version is to be encouraged**. In addition to these, instructor may assign one real life application in the form of a mini-project based on the concepts learned. Instructor may also set one assignment or mini-project that is suitable to respective branch beyond the scope of syllabus.

Suggested List of Laboratory Experiments/Assignments
(Any 2 laboratory assignments to be performed from each group)

Sr. No.	Problem Statement Perform any 2 assignments from each group	CO Mapping
	Group A: Physics of VLSI Devices (24P1201)	
1.	**Carrier Concentration and Fermi-Dirac Distribution(Unit 1)** **Objective:** Analyze the carrier concentrations in intrinsic and extrinsic semiconductors using Fermi-Dirac distribution. • **Tasks:** ○ Implement MATLAB scripts to calculate and plot the carrier concentration as a function of temperature for intrinsic semiconductors. ○ Analyze the Fermi level and carrier concentration in extrinsic semiconductors (n-type and p-type) as a function of doping concentration. ○ Compare the results for direct and indirect semiconductors.	**CO1, CO2**
2.	**Current Flow Mechanisms: Drift and Diffusion Currents (Unit 1)** **Objective:** Simulate and analyze the current flow in semiconductors due to drift and diffusion mechanisms. • **Tasks:** ○ Use MATLAB to simulate drift current density as a function of electric field and carrier mobility. ○ Simulate diffusion current based on concentration gradients. ○ Solve the continuity equation to observe how charge carriers evolve over time in a semiconductor under varying conditions.	**CO1, CO2**
3.	**P-N Junction I-V Characteristics (Unit 2)** **Objective:** Analyze the static current-voltage characteristics of a p-n junction. • **Tasks:** ○ Write a MATLAB code to solve the Poisson equation for a p-n junction under forward and reverse bias conditions.	**CO1, CO2**

	○ Plot the I-V characteristics for both cases and identify the depletion region behavior. ○ Simulate the effect of temperature and doping concentration on the I-V characteristics.	
4.	**MOS Capacitor C-V Characteristics (Unit 3)** **Objective:** Study the capacitance-voltage characteristics of a MOS capacitor in different regions (accumulation, depletion, inversion). • **Tasks:** ○ Develop MATLAB simulations to model the MOS capacitor's C-V characteristics as a function of gate voltage. ○ Explore the effect of oxide thickness and substrate doping concentration on the C-V curve. ○ Discuss how interface charges and oxide charges affect the threshold voltage.	**CO1, CO2**
5.	**Impact of Short Channel Effects on MOSFET Performance (Unit 4)** **Objective:** Simulate short channel effects (SCE) like Drain Induced Barrier Lowering (DIBL) and Punch-through. • **Tasks:** ○ Implement MATLAB models to simulate MOSFET I-V characteristics and observe SCEs such as channel length modulation and DIBL. ○ Analyze the effect of scaling the channel length on device performance (threshold voltage shift, saturation current). ○ Compare the results with long-channel MOSFET behavior.	**CO1, CO2**
6.	**Gate Leakage and Tunneling Effects in UDSM Transistors (Unit 5)** **Objective:** Analyze gate leakage and tunneling effects in ultra-deep submicron (UDSM) transistors. • **Tasks:** ○ Use MATLAB to model gate leakage current as a function of gate oxide thickness for UDSM transistors. ○ Simulate the effect of high-k and low-k dielectrics on gate leakage and threshold voltage. ○ Investigate the impact of tunneling effects on device reliability.	**CO1, CO2**
Group B: Research Methodology (24P1203)		
1.	Use an academic web search to locate a journal paper which describes a design outcome in your field of interest (i.e. your engineering discipline).You must enter several keywords which relate to your topic. Read the paper and, using your own words, demonstrate your understanding of the paper by: Brief Contribution Performance metric, data set, comparative analysis and outcomes **a.** Writing out the major conclusions of the paper **b.** Outlining the verification method(s) used to support these conclusions **c.** Describing the author's reflective comments on the quality of the design (positive and negative). The positive and negative environmental impacts; After reading a published research paper, write down the research question you think the author have addressed in undertaking this research. Do you think the paper adequately supports the conclusions reached in addressing the question?	**CO3, CO4**
2.	Consider a journal article in your discipline that was published approximately five years ago. Note the keywords and type them into one of the web-based academic search engines (e.g. googlescholar.com). Does the original article appear in the search results? How many citations does this article have? Have the same authors published further work in this field?	**CO3, CO4**

3.	Compare the citations of this paper with those from the most highly cited paper in the search results? How many citations does this highly cited article have? If this paper was published before your original article, is it cited in your article? Do you think this high-cited paper should have been listed as a reference in your original article? Give reasons for your decision. Read a journal paper from your discipline. Following the format of patents, write out one or more important outcomes from the paper in terms of one or more Patent Claims 1, 2….. These claims must not only be new, they must be not-obvious from previous work	**CO3, CO4**
4.	**a)** Literature Review Quality: Using a Journal paper selected in your engineering discipline of interest, write a 400-word evaluation of the quality of Literature Review. In particular, review the quality and relevance of cited papers, the comments made on those papers' contribution to the general field, and any omission of papers which are of major importance in the field. **b)** Develop a new research proposal from a published paper: From selected published Journal paper, read the paper. In particular read the discussion and conclusion section and find Suggestions for further work. Apply one of the question words (How? Why? What? When?) and write one or more research questions arising from this paper. This can be used as guide to help you to develop your own research project proposal	**CO3, CO4**
5.	**a)** Download a set of weather data from the Internet covering the temperature and atmospheric pressure over a four-day period. Present the data using 2D and 3D plots, and so deduce if the weather conditions are trending either higher or lower over this four-day period. (Possible web sites include http://www.bom. gov.au/climate/ data/ and http://www.silkeborg-vejret.dk/english/ regn.php).	**CO3, CO4**
6.	**a)** Numerical modeling: Find a paper in which numerical modeling has been used to verify the experimental results. Comment on the differences between the experimental and modeling results. Have the authors commented on the accuracy of the experimental and modeling procedures? What suggestions do you have to improve the quality of the modeling reported in the paper? **b)** Statistical review: In your engineering discipline review a published paper which includes a statistical analysis. Write a brief report on the statistical methods used. Can you suggest an improved statistical analysis? Suggest some additional parameters that might have been measured during the data acquisition stage and so explain how you would analyze the total data set to deduce the influence (and statistical significance) of these additional measurements.	**CO3, CO4**
Group C: Embedded System Design (24P1204)		
1.	**Embedded System Design Using Arduino (Unit 1)** Objective: Learn the basics of embedded system design by exploring the Arduino platform. • **Task:** Set up an Arduino IDE, write a simple C code to read an analog sensor value (e.g., temperature sensor), and display it on an LCD connected to the Arduino. o Install Arduino IDE and set up the development environment. o Interface an analog sensor and LCD with Arduino. o Write a C program to read the sensor data and display it. o Experiment with different sensors and test the real-time behavior.	**CO5, CO6**
2.	**ARM Cortex-M3 GPIO Control using LPC1768 (Unit 2)** Objective: Explore the ARM Cortex-M3 processor, specifically the LPC1768 microcontroller.	**CO5, CO6**

	• **Task:** Write a C program using CMSIS libraries to toggle GPIO pins and control an LED. Set up the LPC1768 microcontroller development environment. o Use CMSIS libraries for GPIO control. o Write and simulate a code to toggle an LED connected to a GPIO pin at regular intervals. o Analyze the behavior using a debugger.	
3.	**STM32 LED Control with STM32CubeIDE (Unit 3)** Objective: Design and implement a basic embedded system using STM32F4XX microcontroller. • **Task**: Write a C code using STM32CubeIDE to toggle an LED with a delay. o Set up STM32CubeIDE for STM32F4XX MCU. o Configure GPIO for LED toggling using STM32CubeMX. o Implement a delay function in the program to control the toggling speed. o Test and validate using the STM32F4 development board.	**CO5, CO6**
4.	**Building an Embedded Linux Kernel (Unit 4)** Objective: Gain experience in building and configuring an embedded Linux kernel. • **Task**: Download and configure a Linux kernel for a specific embedded **platform** (e.g., Raspberry Pi) and boot it using a bootloader. o Use Git to download a specific kernel version from the repository. o Configure the kernel using the appropriate build tools. o Build and deploy the kernel on an embedded system (Raspberry Pi). o Set up the bootloader (U-Boot) and validate the boot process.	**CO5, CO6**
5.	**Automated Meter Reading (AMR) System Design (Unit 5)** Objective: Implement a basic AMR system using a microcontroller and wireless communication protocol. • **Task**: Write a C code to read energy meter data using UART and transmit the data wirelessly using RF modules. o Interface the energy meter with the microcontroller using UART. o Set up the wireless RF module for data transmission. o Write a program to periodically read and transmit the data to a remote system. o Analyze the power consumption of the system.	**CO5, CO6**
6.	**Clap Detection and Counting Using STM32 Microcontroller** Objective: Interface a microphone and a 7-segment LED display with an STM32 microcontroller to detect claps and display the number of claps on the 7-segment display. • **Task**: Write a C program using STM32CubeIDE to detect claps via a microphone input and display the clap count on a 7-segment LED display. o Set up the STM32CubeIDE for the STM32 microcontroller. o Interface the microphone with the STM32 microcontroller to detect sound levels. o Connect and configure a 7-segment LED display to the GPIO pins of the STM32. o Implement a sound detection algorithm to identify claps based on amplitude thresholds. o Write the code to increment the count with each detected clap and display the number of claps on the 7-segment display.	**CO5, CO6**

Matoshri College of Engineering & Research Centre, Nashik
Master of Technology (MTech VLSI & Embedded Systems)

First Year Master of Technology (FY MTech VLSI & Embedded Systems)

24P1207: Elective I Lab

Teaching Scheme	Credit	Examination Head: PR
Practical: 2 Hrs/week	1	Examination Scheme & Marks ISE : 20 Marks ESE: 30 Marks

Course Objectives:

- Understand the principles and applications of microelectromechanical systems (MEMS) and gain hands-on experience in simulating their behavior through various sensors and actuators.
- Equip students with the knowledge and skills to design, implement, and evaluate digital signal processing algorithms using VLSI design techniques, emphasizing performance optimization.
- Develop proficiency in power estimation techniques and low-power design methodologies, enabling students to create energy-efficient integrated circuits.
- Foster skills in developing and implementing FPGA designs using HDL, while enabling students to analyze timing, performance, and resource utilization of their designs.
- Provide students with the capability to implement advanced algorithms in FPGA systems, focusing on optimization techniques to enhance performance and resource efficiency.
- Encourage students to investigate and understand the latest trends and technologies in low-power design, MEMS, and FPGA applications, preparing them for advanced system development challenges.

Course Outcomes:

On completion of the course, learner will be able to:		BL
CO1:	**Analyze** and simulate the behavior of sensors, actuators, and mechanical systems in microelectromechanical applications.	4
CO2:	**Design** and implement digital signal processing algorithms and evaluate their performance in VLSI systems.	6
CO3:	**Apply** power estimation techniques and optimize low-power design methodologies for integrated circuits.	3
CO4:	**Develop** and implement FPGA designs using hardware description languages and analyze their timing and performance characteristics.	4,6
CO5:	**Implement** and optimize complex algorithms in FPGA systems, demonstrating advanced design techniques and methodologies.	3,5
CO6:	**Explore** emerging technologies and trends in low-power design, MEMS, and FPGA applications for advanced system development.	6

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Guidelines for Student's Lab Journal

The laboratory assignments are to be submitted by student in the form of journal. Journal consists of prologue, Certificate, table of contents, and handwritten write-up of each assignment (Title, Objectives, Problem Statement, Outcomes, software & Hardware requirements, Date of Completion, Assessment grade/marks and assessor's sign, Theory-Concept in brief, features of tool/framework/language used, Design, test cases, conclusion. Program codes with sample output of all performed assignments are to be submitted as softcopy.

As a conscious effort and little contribution towards Green IT and environment awareness, attaching printed papers as part of write-ups and program listing to journal may be avoided. Use of DVD containing students programs maintained by lab In-charge is highly encouraged. For reference one or two journals may be maintained with program prints at Laboratory.

Guidelines for Lab /TW Assessment

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Guidelines for Laboratory Conduction

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Suggested List of Laboratory Experiments/Assignments
(Any 5 laboratory assignments to be performed)

Sr. No.	Problem Statement	CO Mapping
	24P1205 (A): Micro Electromechanical Systems	
1.	**Simulation and Analysis of Sensors and Actuators for Micro Motions** *Objective:* Simulate and analyze the behavior of various sensors and actuators to understand their responses to micro-scale motions. • **Task 1:** Select a sensor (e.g., piezoelectric or capacitive sensor) and simulate its response to micro-motion inputs using simulation software. ○ Simulate the behavior of an actuator (e.g., electrostatic or thermal actuator) in response to small displacements. ○ Analyze the correlation between input motion and the sensor/actuator response, focusing on sensitivity and accuracy in detecting micro-motions.	**CO1, CO2**
2.	**Simulation and Analysis of Gear Motion Characteristics** *Objective:* Simulate and analyze the motion characteristics and mechanical principles of gears. • **Task 1:** Create a gear model using simulation software and analyze its rotational motion characteristics. ○ Simulate the interaction between different gear types (spur, helical) and study the effects of varying torque and speed. ○ Evaluate the mechanical efficiency and stress distribution in the gears during operation under load.	**CO1, CO2**
3.	**Demonstration of Hooke's Law Using an Actuator** *Objective:* Demonstrate and understand Hooke's Law by measuring the force exerted by a spring when compressed or extended using an actuator. • **Task 1:** Set up a virtual or physical experiment using a linear actuator to apply a force to a spring and measure the extension/compression. ○ Record the force applied and the corresponding displacement, then plot the force vs. displacement curve to verify Hooke's Law.	**CO1, CO2**

	○ **Task 3:** Analyze the relationship between force and displacement and identify the spring constant for different types of springs.	
4.	**MEMS Packaging and Bonding Techniques** *Objective:* Analyze challenges in MEMS packaging and bonding. • **Task 1:** Compare different bonding techniques (wafer bonding, anodic bonding, fusion bonding) and their application in MEMS packaging. ○ Research challenges in packaging MEMS devices and propose solutions for high-reliability packaging. ○ Write a report on advancements in MEMS packaging technologies.	**CO1, CO6**
5.	**Sensor Design and Simulation** *Objective:* Design and simulate pressure sensors and accelerometers. • **Task 1:** Use FEA software to model a MEMS pressure sensor, analyzing its mechanical properties. ○ Design an accelerometer in simulation software and analyze its performance in different conditions (e.g., varying pressure). ○ Compare the performance of different MEMS sensors (e.g., gyroscopes, biosensors) using simulation.	**CO1, CO6**
6.	**MEMS RF Devices and Case Studies** *Objective:* Analyze RF MEMS devices, such as switches and resonators. • **Task 1:** Simulate a MEMS switch using RF software tools and study its switching behavior. ○ Design a MEMS resonator and analyze its frequency response. ○ Write a case study on the application of RF MEMS in telecommunications.	**CO1, CO6**
24P1205 (B): VLSI Digital Signal Processing		
1.	**DSP System Design and Algorithm Simulation** *Objective:* Implement and simulate basic DSP algorithms using VLSI design principles. • **Task:** Design and simulate a basic FIR filter using MATLAB or Python. ○ Simulate an IIR filter and compare its performance to the FIR filter. ○ Analyze the power and performance trade-offs for both filters when implemented in VLSI architectures.	**CO2, CO4**
2.	**Pipelining and Parallel Processing in DSP Systems** *Objective:* Implement pipelining and parallel processing techniques in DSP systems for performance optimization. • **Task:** Design a simple DSP system with basic pipelining for a FIR filter. ○ Implement parallel processing for the same system and compare the latency and throughput improvements. ○ Analyze the impact of pipelining and parallelism on power consumption and performance.	**CO2, CO4**
3.	**VLSI Implementation of FFT Algorithm** *Objective:* Implement the Fast Fourier Transform (FFT) algorithm in VLSI and analyze its performance. • **Task:** Design and simulate a 4-point FFT using HDL (Verilog/VHDL). ○ Implement the FFT in hardware using FPGA or ASIC and measure the performance. ○ Evaluate the power consumption of the FFT implementation for real-time DSP applications.	**CO2, CO4**
4.	**VLSI Implementation of Discrete Cosine Transform (DCT)** *Objective:* Implement the DCT algorithm in VLSI for applications in image and video processing.	**CO2, CO5**

	• **Task:** Write HDL code to implement the 2D DCT algorithm and simulate its performance. ○ Optimize the design for low-power and high-performance applications. ○ Analyze the computational complexity and power consumption of the DCT algorithm.	
5.	**Adaptive Filter Implementation (LMS Algorithm)** *Objective:* Implement the LMS adaptive filtering algorithm on VLSI for noise cancellation applications. • **Task:** Design and simulate the LMS adaptive filter using HDL (Verilog/VHDL). ○ Implement the filter on FPGA or ASIC and validate its performance in noise-cancellation tasks. ○ Evaluate the power and area trade-offs for the adaptive filter implementation.	**CO2, CO5**
6.	**Neuromorphic Computing and DSP Applications** *Objective:* Explore neuromorphic computing concepts in DSP and implement a simple neural network on VLSI. • **Task:** Implement a basic feedforward neural network for pattern recognition using HDL. ○ Simulate and analyze the performance of the neural network in comparison to traditional DSP algorithms. ○ Investigate the power consumption and scalability of neuromorphic computing architectures in VLSI.	**CO2, CO6**
24P1205 (C): Low Power IC Design		
1.	**Power Estimation Techniques in Digital Circuits** *Objective:* Estimate power dissipation in digital circuits using various power estimation techniques. • **Task:** Simulate a simple digital circuit (e.g., a full adder) and estimate its dynamic, static, and short-circuit power dissipation using gate-level techniques. ○ Perform RTL-level power estimation on a small processor core and compare with gate-level results. ○ Use system-level power estimation tools to analyze power efficiency metrics such as energy per operation and power-delay product.	**CO3, CO5**
2.	**Transistor Sizing and Power Optimization** *Objective:* Optimize transistor sizing for power efficiency in CMOS circuits. • **Task:** Implement and simulate a CMOS inverter and vary transistor sizes to minimize dynamic and leakage power dissipation. ○ Analyze the impact of transistor sizing on circuit speed and power-delay product. ○ Experiment with different CMOS logic gates (e.g., NAND, NOR) to understand the effects of transistor sizing on power and performance.	**CO3, CO5**
3.	**Dynamic Voltage and Frequency Scaling (DVFS)** *Objective:* Explore DVFS techniques to reduce power consumption in digital systems. • **Task:** Simulate a processor core with different voltage and frequency levels using Verilog/VHDL and observe power reduction. ○ Analyze the trade-offs between performance and power using DVFS in real-time workloads. ○ Implement a power-aware system that dynamically scales voltage and frequency based on workload requirements.	**CO3, CO6**

4.	**Power Gating and Multi-Threshold CMOS Design** *Objective:* Implement power gating and multi-threshold CMOS techniques to reduce leakage power. • **Task:** Design a simple digital circuit (e.g., a counter) with power gating and simulate the reduction in leakage power using SPICE. ○ Compare the performance and power dissipation of the design with and without power gating under various load conditions. ○ Implement multi-threshold CMOS design in the same circuit and analyze the leakage power reduction.	**CO3, CO6**
5.	**Low Power Memory Design** *Objective:* Design low-power SRAM and explore leakage reduction techniques in memory circuits. • **Task:** Implement a 4x4 SRAM cell and simulate its power consumption in active and standby modes. ○ Apply leakage power reduction techniques like reverse body biasing and stack forcing to minimize standby power. ○ Compare power consumption of SRAM with DRAM and non-volatile memories for different read/write operations.	**CO3, CO6**
6.	**Exploring Emerging Low-Power Technologies** *Objective:* Explore emerging low-power technologies like FinFETs, TFETs, and NEM relays. • **Task:** Simulate a basic logic circuit using FinFET technology and compare its power consumption with traditional CMOS technology. ○ Design and simulate a basic TFET-based inverter and analyze its power characteristics. ○ Research NEM relays and propose a power-efficient circuit design for ultra-low-power applications (e.g., biomedical devices).	**CO3, CO6**
24P1205 (D): System Design with FPGA		
1.	**FPGA Architecture Exploration Using HDL** *Objective:* Understand the FPGA architecture and develop basic designs using HDLs. • **Task:** Create a simple combinational logic circuit (e.g., an AND gate and a multiplexer) using Verilog/VHDL. ○ Implement the design on a Xilinx/Intel FPGA board and analyze the usage of CLBs, IOBs, and routing resources. ○ Perform timing analysis and verify the design using simulation tools (Xilinx Vivado or Intel Quartus Prime).	**CO4, CO5**
2.	**FPGA Design Flow and Tool Exploration** *Objective:* Explore the FPGA design flow using industry-standard FPGA tools. • **Task:** Design a 4-bit counter using Verilog/VHDL and simulate the design in Xilinx Vivado or Intel Quartus Prime. ○ Perform synthesis, place and route, and implementation steps in the FPGA design flow. ○ Verify the design by downloading it to an FPGA board and observing the output using LEDs or a logic analyzer.	**CO4, CO5**
3.	**Timing Analysis and Constraints in FPGA Designs** *Objective:* Implement and verify FPGA timing constraints and perform timing analysis. • **Task:** Implement a basic sequential circuit (e.g., a shift register) and analyze its timing characteristics.	**CO4, CO5**

	○ Apply design constraints using the Xilinx Constraints File (XCF) or Intel's SDC format and evaluate timing performance. ○ Optimize the design to meet timing requirements and verify it on the FPGA board.	
4.	**FPGA-Based Embedded System Design** *Objective:* Design and implement an embedded system on FPGA using an ARM-based SoC. • **Task:** Integrate a MicroBlaze processor on a Xilinx FPGA or Nios II processor on an Intel FPGA. ○ Interface the processor with external peripherals like UART, GPIO, and SPI. ○ Develop and execute a simple program to control LEDs and switches using the embedded processor.	**CO4, CO5**
5.	**High-Level Synthesis (HLS) for FPGA Design** *Objective:* Use high-level synthesis (HLS) tools for FPGA design optimization. • **Task:** Design a simple FIR filter using C/C++ code and synthesize it for FPGA using HLS tools (e.g., Xilinx Vivado HLS). ○ Compare the performance and resource utilization of the HLS-generated design with a manually written HDL design. ○ Analyze the trade-offs between performance, area, and power for different optimization settings.	**CO4, CO5**
6.	**FPGA-Based System Prototyping and Peripheral Interfacing** *Objective:* Prototype a system using FPGA and interface with external peripherals. • **Task:** Design an FPGA-based system that interfaces with external peripherals such as ADCs, DACs, or sensors (e.g., temperature or light sensors). ○ Implement communication protocols such as I2C or SPI to interface with the peripherals. ○ Test the system by reading sensor data and displaying it on an LCD or sending it over UART to a PC.	**CO4, CO5**

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Home

24P1208: Study of Indian Constitution

Teaching Scheme	Credit	Examination Head: SEMI
Tutorial: 1 Hr/week	1	Examination Scheme & Marks ISE : 20 Marks ESE: 30 Marks
Prerequisite:	Any graduate	

Course Objectives:

- To acquaint with the basic principles of Constitution and Constitutionalism
- To understand the reasons, operation and justification of the growth of Fundamental Rights in India
- To learn the Directive Principles of India.
- To understand the powers, functions and structures of various Constitutional bodies.
- To study the constitutional operations in the context of social, economic and political.

Course Outcomes:

On completion of the course, learner will be able to:		BL
CO1:	**Apply** knowledge of the historical background, key features, and provisions related to citizenship in the Indian Constitution to assess its relevance to contemporary governance.	3
CO2:	**Analyze** and present findings for study of - the structure and classification of fundamental rights, directive principles of state policy, and fundamental duties enshrined in the Constitution.	6
CO3:	**Comprehend** the roles, powers, and functions of the Union executive, Union Legislature, and Union judiciary, with a focus on parliamentary procedures and the Supreme Court.	2
CO4:	**Survey** the composition, powers, and functions of the State executive, State Legislature, and State judiciary, including the role of Governors and High Courts.	4
CO5:	**Discover** the legislative, administrative, and financial relations between the Union and State governments, including provisions for emergency, trade, and amendments to the Constitution.	4
CO5:	**Elaborate** the Indian Constitution's framework and its role in governing the structure and functioning of both the Union and State governments, fostering responsible citizenship.	6

Unit-I:	Introduction and Citizenship	4 hrs

Definition of constitution, historical back ground, salient features of the constitution. Preamble of the constitution, union and its territory. Meaning of citizenship, types, termination of citizenship.

Unit-II:	Rights in the Constitution and Directive principles of state policy	6 hrs

Definition of state, fundamental rights, general nature, classification, right to equality, right to freedom, right against exploitation. Right to freedom of religion, cultural and educational rights, right to constitutional remedies. Protection in respect of conviction for offences. Directive principles of state policy, classification of directives, fundamental duties.

Unit-III:	**Structure, Powers and Functions of Union Legislature**	**5 hrs**
The Union executive, the President, the vice President, the council of ministers, the Prime minister, Attorney-General, functions. The parliament, composition, Rajya Sabha, Lok Sabha, qualification and disqualification of membership, functions of parliament. Union judiciary, the supreme court, jurisdiction, appeal by special leave.		
Unit-IV:	**Structure, Powers and Functions of State Legislature**	**5 hrs**
The State executive, the Governor, the council of ministers, the Chief minister, advocate general, union Territories. The State Legislature, composition, qualification and disqualification of membership, functions. The state judiciary, the high court, jurisdiction, writs jurisdiction.		
Unit-V:	**Legislative relation between Union and State**	**5 hrs**
Relations between the Union and the States, legislative relation, administrative relation, financial Relations, Inter State council, finance commission. Emergency provision, freedom of trade commerce and inter course, comptroller and auditor general of India, public Services, public service commission, administrative Tribunals. Official language, elections, special provisions relating to certain classes, amendment of the Constitution.		
Text Books:		
1]. **"Introduction to the constitution of India",** D. D. Basu, Lexis Nexis, New Delhi, 24e, 2019 2]. **"The constitution of India, Universal Law",** P. M. Bhakshi, , 14e, 2017		
Reference Books:		
1]. **"The constitution of India",** Ministry of law and justice, Govt of India, New Delhi, 2019. 2]. **"The constitutional law of India**", Dr. J. N. Pandey, Allahabad, 51e, 2019 3]. **"India's Constitution",** M. V. Pylee, S Chand and company, New Delhi, 16e, 2016		

The CO-PO Mapping Matrix:

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2
CO1	-	2	2	-	-	1	-	-
CO2	-	2	-	-	-	2	-	-
CO3	-	3	2	-	-	2	-	-
CO4	-	2	-	-	-	1	-	-
CO5	-	3	2	-	--	1	-	-
CO6	-	2	-	-		2	-	-

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